Amendments to the Specification:

Please replace paragraphs 37, 65 and 69 presently on file with those set forth below:

[037] As noted above, noise is one of the most common problems associated with charge pumps. FIGURE 3 illustrates an exemplary charge pump architecture, showing some of the paths in which noise currents may typically occur. The charge pump of FIGURE 3 includes a transfer capacitor C_T 202, together with source supply connections Vs+ 208 and Vs- 210, which are substantially as shown in FIGURE 2, and accordingly are identically numbered. FIGURE 3 also includes output supply connections Vo+ 316 and Vo- 318. The fly capacitor coupling switches, which couple C_T 202 to the source supply Vs or to the output supply Vo, are shown as MOSFET devices controlled by a signal applied to a control node (the device gate). The fly capacitor coupling switches include a P-channel switch 304 under control of a first clock output 354, a P-channel switch 306 under control of a second clock output 356, an N-channel switch [[312]] **314** under control of a third clock output 362, and an N-channel switch [[314]] **312** under control of a fourth clock output 364. The four charge pump clock outputs (354, 356, 362, and 364) are generated in a charge pump clock generator circuit 350. A filter capacitor 330 for the output supply Vo, as well as a current load 332 on Vo, are also shown.

[065] The circuit of FIGURE 9 may also be configured to produce negative voltages. Vh 920 may be connected to a positive source voltage Vs+, while Vg 918 and Ve 914 are connected to a reference (ground) voltage, to produce -(Vs+) at Vf 916. Vc 908 and Va 904 may be connected to Vf 916. An output Vb 906 will be approximately -2*Vs+ if Vd 910 is connected to ground. If, instead, Vd 910 is connected to Vs+, then [[Vd 910]] output Vb 906 will be driven to approximately -3*Vs+. Capacitive storage, not shown, is assumed for each supply and intermediate voltage.

[069] FIGURE 10 is a simplified schematic diagram that illustrates generation of arbitrary voltages by means of charge pump techniques. A source voltage Vs+ 1002 may be used to derive an intermediate voltage, for example by means of resistors 1004 and 1006. Such intermediate voltage may optionally be buffered, if significant current output is desired, by means of buffer amplifier 1008, or may at least be connected to ground via a decoupling capacitor (not shown), to produce a projection voltage 1010 (with respect to common, or ground). The projection voltage 1010 may be regulated, for example by means of feedback (not shown) applied to amplifier 1008. P-switches 800 and n-switches 830 may be employed in conjunction with a fly capacitor 1012, as shown. Vb may be an available voltage source (*e.g.*, Vs+).

Operation of the circuit will establish Va 1014 at a voltage approximately equal to that of Vb [[1017]] 1016 plus the projection voltage 1010. The skilled person will readily see that rearrangement of the circuit will permit generation of arbitrary negative voltages with equal simplicity. Larger voltages may be obtained by stacking charge pump circuits, in a manner as described with respect to FIGURE 9. Thus, arbitrary positive or negative voltages may be generated by means of charge pump circuits. All such charge pump circuits may be controlled by a single phase of a clock. Of course, the switches associated with different fly capacitors may alternatively use different clocks for control. Active switches may also be replaced with passive switches, for example in a manner as described with respect to FIGURE 7 or FIGURE 9.

Please replace the abstract presently on file with the abstract set forth below:

A charge pump method and apparatus is described having various aspects. Noise injection from a charge pump to other circuits may be reduced by limiting both positive and negative clock transition rates, as well as by limiting drive currents within clock generator driver circuits, and also by increasing a control node AC impedance of certain transfer capacitor coupling switches. A single-phase clock may be used to control as many as all active switches within a charge pump, and capacitive coupling may simplify biasing and timing for clock signals controlling transfer capacitor coupling switches. Any combination of such aspects of the method or apparatus may be employed to quiet and/or simplify charge pump designs over a wide range of charge pump architectures.